



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/577,666	05/01/2006	Toshihisa Nagata	R2184.0492/P492	8451
24998	7590	11/24/2009		
DICKSTEIN SHAPIRO LLP 1825 EYE STREET NW Washington, DC 20006-5403			EXAMINER BEHM, HARRY RAYMOND	
			ART UNIT 2838	PAPER NUMBER
			MAIL DATE 11/24/2009	DELIVERY MODE PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	<b>Application No.</b> 10/577,666	<b>Applicant(s)</b> NAGATA ET AL.	
	<b>Examiner</b> HARRY BEHM	<b>Art Unit</b> 2838	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 01 October 2009.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1-11 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-11 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |   |   |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)                    | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____                                      |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)         | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____   | 6) <input type="checkbox"/> Other: _____                          |

## **DETAILED ACTION**

### ***Response to Arguments***

Applicant's arguments filed 10/1/09 have been fully considered but they are not persuasive. Applicant argues Devore does not teach or suggest that the sense transistor 18 includes the sense transistors 38, 40, 42 and 44 connected in parallel. However, this is not found persuasive since Devore explicitly discloses transistors 38, 40, 42 and 44 are the sense transistors and one of ordinary skill would recognize the sense transistors must be connected in parallel. The sense transistors function by mirroring the current through the power transistor 26 and must be placed in parallel to form the current mirror ("Transistors 40, 42, and 44 are identical in construction to transistor 38. Transistors 38, 40, 42, and 44 are proportionate in size to transistor 26 and are constructed using the same processes that are used to construct the components of transistor 26. As such, transistors 38, 40, 42, and 44 can be used to track and control the amount of current provided by transistor 26", column 5, lines 4-9). At the time of the invention it was well known to form a transistor from smaller transistors connected in parallel. Furthermore Devore discloses "the signals from these sense transistors may be effectively averaged using conventional techniques to provide for an average value of the current passing through all the sense transistors" (column 3, lines 22-26) so it remains clear the sense transistors must be connected in parallel.

Applicant argues claims 2-11 are allowable for the same reasons as claim 1, but claim 1 is not allowable as indicated.

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-4 are rejected under 35 U.S.C. 102(b) as being anticipated by Devore (US 5,408,141).

With respect to Claim 1, Devore discloses a semiconductor device comprising a semiconductor chip (Fig. 3 25); a driver transistor (Fig. 3 26) mounted on said semiconductor chip; a monitor transistor (Fig. 1 18) for detecting electric current flowing in said driver transistor; and a plurality of transistors (Fig. 3 38,40,42,44) provided in the monitor transistor and connected in parallel; wherein the plural transistors (Fig. 3 38,40,42,44) are disposed at a periphery of an area of the semiconductor chip (Fig. 3 25) on which the driver transistor (Fig. 3 26) is mounted; such that the plural transistors (Fig. 3 38,40,42,44) are located around a center portion of the area of the semiconductor chip on which the driver transistor is mounted, and are not located (Fig. 3 38,40,43,44 not in center) in the center portion of the area of the semiconductor chip on which the driver transistor is mounted, such that the monitor transistor (Fig. 1 18) is not located in the center portion of the area since the monitor transistor is distributed throughout the semiconductor chip on which the driver transistor is mounted; and wherein the plural transistors (Fig. 3 38,40,43,44) are located relative to the semiconductor chip and the driver transistor such that changes in a property of the

Art Unit: 2838

monitor transistor caused when force is applied to the semiconductor chip are balanced since the plural transistors are symmetrically distributed around the periphery the change in property will be balanced due to averaging.

With respect to Claim 2, Devore discloses a semiconductor device as set forth above wherein the plural transistors (Fig. 3 38,40,43,44) are disposed within an area (Fig. 3 26) of the semiconductor chip (Fig. 3 25) on which the drive transistor is mounted.

With respect to Claim 3, Devore discloses a semiconductor device as set forth above wherein the plural transistors (Fig. 3 38,40,43,44) are disposed on the semiconductor chip (Fig. 3 25) at equal intervals.

With respect to Claim 4, Devore discloses the semiconductor device as set forth above wherein the driver transistor (Fig. 3 25) and the monitor transistors (Fig. 3 38,40,43,44) are MOS transistors ("FIG. 3 illustrates an exemplary lateral MOS configuration", column 4, lines 16-17).

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 5-8 and 10-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miller (US 6,734,656) in view of Devore (US 5,408,141).

With respect to Claim 5, Miller discloses a voltage regulator (Fig. 7) provided with a constant voltage circuit part ("reference voltage supply" column 3, lines 60-64) including a driver transistor (Fig. 7 730) mounted on a semiconductor chip and an output current detection circuit part including a monitor transistor (Fig. 8 730-M) for detecting electric current flowing in the driver transistor (Fig. 8 730-(N-M)), the voltage regulator comprising a plurality of transistors (Fig. 8 M) provided in the monitor transistor and connected in parallel. Miller does not disclose the layout of the monitor transistors. Devore discloses a semiconductor device comprising a semiconductor chip (Fig. 3 25); a driver transistor (Fig. 3 26) mounted on said semiconductor chip; a monitor transistor (Fig. 1 18) for detecting electric current flowing in said driver transistor; and a plurality of transistors (Fig. 3 38,40,43,44) provided in the monitor transistor and connected in parallel; wherein the plural transistors (Fig. 3 38,40,43,44) are disposed at a periphery of an area of the semiconductor chip (Fig. 3 25) on which the driver transistor (Fig. 3 26) is mounted; such that the plural transistors (Fig. 3 38,40,42,44) are located around a center portion of the area of the semiconductor chip on which the

Art Unit: 2838

driver transistor is mounted, and are not located (Fig. 3 38,40,43,44 not in center) in the center portion of the area of the semiconductor chip on which the driver transistor is mounted, such that the monitor transistor (Fig. 1 18) is not located in the center portion of the area since the monitor transistor is distributed throughout the semiconductor chip on which the driver transistor is mounted; and wherein the plural transistors (Fig. 3 38,40,43,44) are located relative to the semiconductor chip and the driver transistor such that changes in a property of the monitor transistor caused when force is applied to the semiconductor chip are balanced since the plural transistors are symmetrically distributed around the periphery the change in property will be balanced due to averaging. It would have been obvious to one of ordinary skill in the art at the time of the invention to position the monitor transistors at the periphery of an area of the driver transistor. The reason for doing so was to eliminate "the effects of thermal gradients over the operation of the integrated device. As such, the sense device can accurately track the current output by the entire power device" (Devore column 2, lines 4-7).

With respect to Claims 6-7, Miller in view of Devore disclose the voltage regulator as set forth above. See claims 2 and 3, respectively, for additional details.

With respect to Claim 8, Miller in view of Devore disclose the voltage regulator as set forth above, wherein the output current detection circuit part (Fig. 8 770) is configured to change the electric current flowing in the monitor transistor into electric voltage and output the electric voltage (Fig. 7  $V_{out}$  at 755).

With respect to Claim 10, Miller in view of Devore disclose the voltage regulator as set forth above. See claim 4 for additional details.

With respect to Claim 11, Miller in view of Devore disclose the voltage regulator as set forth above, wherein the constant voltage circuit part and the output current detection circuit part are integrated on a single integrated circuit (Devore Fig. 3 25).

Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Miller (US 6,734,656) in view of Devore (US 5,408,141) further in view of Zadeh (US 6,522,111).

With respect to Claim 9, Miller in view of Devore disclose the voltage regulator as set forth above, wherein the constant voltage circuit part further includes a reference voltage generation circuit ("reference voltage supply", Miller column 3, lines 63-64) for generating and outputting a reference voltage and an operational amplifier circuit ("error amplifier circuitry 712", Miller column 3, lines 61-62) including a differential pair for controlling the operation of the driver transistor (Miller Fig. 7 730), wherein the output current detection is supplied to the controller (Fig. 710). Miller does not detail how the controller uses the current feedback. Zadeh teaches adaptive biasing wherein the output current detection circuit part (Fig. 2 214) is configured to supply an electric current to the differential pair of the operational amplifier circuit (Fig. 2 218), wherein the electric current supplied to the differential pair is proportional to the electric current flowing in the monitor transistor. It would have been obvious to one of ordinary skill in the art at the time of the invention to provide the proportional electric current to the



Art Unit: 2838

operational amplifier. The reason for doing so was to provide adaptive biasing and "thereby improving transient responses" (Zadeh column 2, lines 7-8).

### ***Conclusion***

**THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to **HARRY BEHM** whose telephone number is (571)272-8929. The examiner can normally be reached on 7:00 am - 4:00 pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Monica Lewis can be reached on (571) 272-1838. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2838

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Harry Behm/  
Examiner, Art Unit 2838